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APPLICATION NO.	FILIN	IG DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO. CONFIRMATION NO.		
09/817,193	03/2	27/2001	Masahiko Tsuchiya	108097	9085	
25944	7590	01/03/2003				
OLIFF & BERRIDGE, PLC				EXAMINER		
P.O. BOX 19 ALEXANDE		2320		TRA, ANH QUAN		
				ART UNIT	PAPER NUMBER	
	•			2816	<u> </u>	
				DATE MAILED: 01/03/2003		

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)	
Advisory Action	09/817,193	TSUCHIYA, MASAHIKO	
,	Examiner	Art Unit	
	Quan Tra	2816	
The MAILING DATE of this communication ap	opears on the cover sheet w	vith the correspondence address	
THE REPLY FILED 09 December 2002 FAILS TO PL Therefore, further action by the applicant is required to final rejection under 37 CFR 1.113 may only be either: condition for allowance; (2) a timely filed Notice of App Examination (RCE) in compliance with 37 CFR 1.114.	avoid abandonment of thi	s application. A proper reply to a	
PERIOD FOR	REPLY [check either a) or	b)]	
 a)	nis Advisory Action, or (2) the dat ire later than SIX MONTHS from VAS FILED WITHIN TWO MONT	the mailing date of the final rejection. THS OF THE FINAL REJECTION. See MPER	Р
Extensions of time may be obtained under 37 CFR 1.136(a). The fee have been filed is the date for purposes of determining the period fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date (2) as set forth in (b) above, if checked. Any reply received by the (1) timely filed, may reduce any earned patent term adjustment. See 3	od of extension and the correspo of the shortened statutory perion Office later than three months aft	nding amount of the fee. The appropriate extending amount of the fee.	tension
 A Notice of Appeal was filed on Appellar CFR 1.192(a), or any extension thereof (37 C 	nt's Brief must be filed with CFR 1.191(d)), to avoid dis	in the period set forth in missal of the appeal.	
2. The proposed amendment(s) will not be entered	l because:		
(a) they raise new issues that would require fur	ther consideration and/or	search (see NOTE below);	
(b) they raise the issue of new matter (see Not	e below);		
(c) they are not deemed to place the applicatio issues for appeal; and/or	n in better form for appeal	by materially reducing or simplifying	the
(d) ☐ they present additional claims without cand NOTE:	celing a corresponding nun	nber of finally rejected claims.	
3. Applicant's reply has overcome the following reje	ection(s):		
4. Newly proposed or amended claim(s) wou canceling the non-allowable claim(s).	uld be allowable if submitte	d in a separate, timely filed amendm	ent
5.⊠ The a)☐ affidavit, b)☐ exhibit, or c)⊠ request application in condition for allowance because:	for reconsideration has be <u>See Continuation Sheet</u> .	en considered but does NOT place th	he
6. The affidavit or exhibit will NOT be considered b raised by the Examiner in the final rejection.		OLELY to issues which were newly	
7. For purposes of Appeal, the proposed amendme explanation of how the new or amended claims	ent(s) a)⊠ will not be ente would be rejected is provi	red or b) will be entered and an ded below or appended.	
The status of the claim(s) is (or will be) as follow	s:		
Claim(s) allowed:			
Claim(s) objected to:			
Claim(s) rejected: 1-9.			
Claim(s) withdrawn from consideration:			
8. The proposed drawing correction filed on	is a) ☐ approved or b) ☐	disapproved by the Examiner	
9. Note the attached Information Disclosure Statem			
0. Other:	(5)(1 10-1445) I apel	Terryb. Cunning Primary Exami	3

Continuation of 5. does NOT place the application in condition for allowance because:

In response to Applicant's arguments in page 3, second paragraph, of the remarks, Andrews teaches in column 1, third paragraph that "The transistors in the differential pair also have widths ratios of 1:5". Therefore, the transistors in the differential pair having difference driving ability because they have difference widths.

In response to Applicant's arguments in page 4, second paragraph, figures 1 and 2 show the first differential circuit outputs the first signal (Vout from 0 mS to 0.45 mS) in order to output the first output votlage lower than the common input votlage (VIN) through the third transistor (P4) of the primary conductive type, and the second differential circuit outputs the second signal (Vout from 0.5 mS. to 1 mS) in order to output a second output votlage higher than the common input votlage (VIN) through the third transistor (N4) of the secondary conductive type.

In response to Applicant's arguments in pages 5 and 6, Seller fails to teach at least one of the first differntial pair and the second differential pair is formed from a pair of transistors having a driving ability difference therebetween. However, Shulman teaches in column 5, that the size of transistors in differntial pair can be differentent in order to have off-set for the amplifier. Therefore, it would have been obvious to one having ordinary skill in the art to employ Shulman's teaching to realize the transistors in Saller et al.'s differntial pair for the purpose of having off-set for the amplifier. Regtarding to Applicant's statement in page 5, fourth paragraph, the final office action does not indicate that Shulman's teaching would be inherent in Seller. The final office action states that "it would have been obvious to one having ordinary skill in the art to make the size of transistors in Saller et al. differntial pair to be different for the purpose o having off-set for the amplifier".